DACSINE PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - Apps www.analog.com/MicroConverter

4 ;

5 ; Date : 3 April 2002

6 ;

7 ; File : DACsine.asm

8 ;

9 ; Hardware : ADuC832

10 ;

11 ; Description : Outputs a sine waves on DAC0 at 1.09kHz.

12 ; Rate calculations assume a 16.777216 Mclk, pllcon=0

13 ;

14 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

15

16 $MOD832 ; Use 8052&ADuC832 predefined symbols

17

00B4 18 LED EQU P3.4 ; P3.4 drives red LED on eval board

19

20 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

21 ; BEGINNING OF CODE

---- 22 CSEG

23

0000 24 ORG 0000h

0000 75EF80 25 MOV ADCCON1,#80H

0003 75D700 26 MOV PLLCON,#00h

0006 75FD0D 27 MOV DACCON,#00Dh ; DAC0 on, 12bit, asynchronous

0009 75FA08 28 MOV DAC0H,#008h

000C 75F900 29 MOV DAC0L,#000h ; DAC0 to mid-scale

30

000F 901000 31 MOV DPTR,#TABLE

32

0012 E4 33 STEP: CLR A ; 1

0013 93 34 MOVC A,@A+DPTR ; get high data byte from table.. 2

0014 F5FA 35 MOV DAC0H,A ; ..and move it into DAC register 1

0016 A3 36 INC DPTR ; move on to get low byte 2

37

0017 E4 38 CLR A ; 1

0018 93 39 MOVC A,@A+DPTR ; get low data byte from table.. 2

0019 F5F9 40 MOV DAC0L,A ; ..and update DAC output 1

001B A3 41 INC DPTR ; move on for next data point 2

42

001C 53827F 43 ANL DPL,#07Fh ; wrap around at end of table 2

44

001F E5FA 45 MOV A,DAC0H ; 1

0021 A2E3 46 MOV C,ACC.3 ; MSB of DAC0 value 1

0023 92B4 47 MOV LED,C ; LED = MSB of DAC0 2

48

0025 80EB 49 JMP STEP ; 2

50

51 ; numbers at right in the above loop represent the number of machine

52 ; cycles for each instruction. the complete loop takes exactly 20

53 ; machine cycles. with an 16.777216MHz master clock, a machine cycle

54 ; is 715ns, so the above loop takes 14.30us to update each data

55 ; point. since there are 64 data points in the below sine lookup

56 ; table, this results in a 0.915ms period, i.e. a 1.09KHz frequency.

57

58 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

DACSINE PAGE 2

59 ; SINE LOOKUP TABLE

1000 60 ORG 01000h

61

1000 62 TABLE:

63

1000 07FF 64 DB 007h, 0FFh

1002 08C8 65 DB 008h, 0C8h

1004 098E 66 DB 009h, 08Eh

1006 0A51 67 DB 00Ah, 051h

1008 0B0F 68 DB 00Bh, 00Fh

100A 0BC4 69 DB 00Bh, 0C4h

100C 0C71 70 DB 00Ch, 071h

100E 0D12 71 DB 00Dh, 012h

1010 0DA7 72 DB 00Dh, 0A7h

1012 0E2E 73 DB 00Eh, 02Eh

1014 0EA5 74 DB 00Eh, 0A5h

1016 0F0D 75 DB 00Fh, 00Dh

1018 0F63 76 DB 00Fh, 063h

101A 0FA6 77 DB 00Fh, 0A6h

101C 0FD7 78 DB 00Fh, 0D7h

101E 0FF5 79 DB 00Fh, 0F5h

1020 0FFF 80 DB 00Fh, 0FFh

1022 0FF5 81 DB 00Fh, 0F5h

1024 0FD7 82 DB 00Fh, 0D7h

1026 0FA6 83 DB 00Fh, 0A6h

1028 0F63 84 DB 00Fh, 063h

102A 0F0D 85 DB 00Fh, 00Dh

102C 0EA5 86 DB 00Eh, 0A5h

102E 0E2E 87 DB 00Eh, 02Eh

1030 0DA7 88 DB 00Dh, 0A7h

1032 0D12 89 DB 00Dh, 012h

1034 0C71 90 DB 00Ch, 071h

1036 0BC4 91 DB 00Bh, 0C4h

1038 0B0F 92 DB 00Bh, 00Fh

103A 0A51 93 DB 00Ah, 051h

103C 098E 94 DB 009h, 08Eh

103E 08C8 95 DB 008h, 0C8h

1040 07FF 96 DB 007h, 0FFh

1042 0736 97 DB 007h, 036h

1044 0670 98 DB 006h, 070h

1046 05AD 99 DB 005h, 0ADh

1048 04EF 100 DB 004h, 0EFh

104A 043A 101 DB 004h, 03Ah

104C 038D 102 DB 003h, 08Dh

104E 02EC 103 DB 002h, 0ECh

1050 0257 104 DB 002h, 057h

1052 01D0 105 DB 001h, 0D0h

1054 0159 106 DB 001h, 059h

1056 00F1 107 DB 000h, 0F1h

1058 009B 108 DB 000h, 09Bh

105A 0058 109 DB 000h, 058h

105C 0027 110 DB 000h, 027h

105E 0009 111 DB 000h, 009h

1060 0000 112 DB 000h, 000h

1062 0009 113 DB 000h, 009h

1064 0027 114 DB 000h, 027h

1066 0058 115 DB 000h, 058h

1068 009B 116 DB 000h, 09Bh

DACSINE PAGE 3

106A 00F1 117 DB 000h, 0F1h

106C 0159 118 DB 001h, 059h

106E 01D0 119 DB 001h, 0D0h

1070 0257 120 DB 002h, 057h

1072 02EC 121 DB 002h, 0ECh

1074 038D 122 DB 003h, 08Dh

1076 043A 123 DB 004h, 03Ah

1078 04EF 124 DB 004h, 0EFh

107A 05AD 125 DB 005h, 0ADh

107C 0670 126 DB 006h, 070h

107E 0736 127 DB 007h, 036h ; end of table

128

129 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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131 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

DACSINE PAGE 4

ACC. . . . . . . . . . . . . . . D ADDR 00E0H PREDEFINED

ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

DAC0H. . . . . . . . . . . . . . D ADDR 00FAH PREDEFINED

DAC0L. . . . . . . . . . . . . . D ADDR 00F9H PREDEFINED

DACCON . . . . . . . . . . . . . D ADDR 00FDH PREDEFINED

DPL. . . . . . . . . . . . . . . D ADDR 0082H PREDEFINED

LED. . . . . . . . . . . . . . . NUMB 00B4H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

PLLCON . . . . . . . . . . . . . D ADDR 00D7H PREDEFINED

STEP . . . . . . . . . . . . . . C ADDR 0012H

TABLE. . . . . . . . . . . . . . C ADDR 1000H